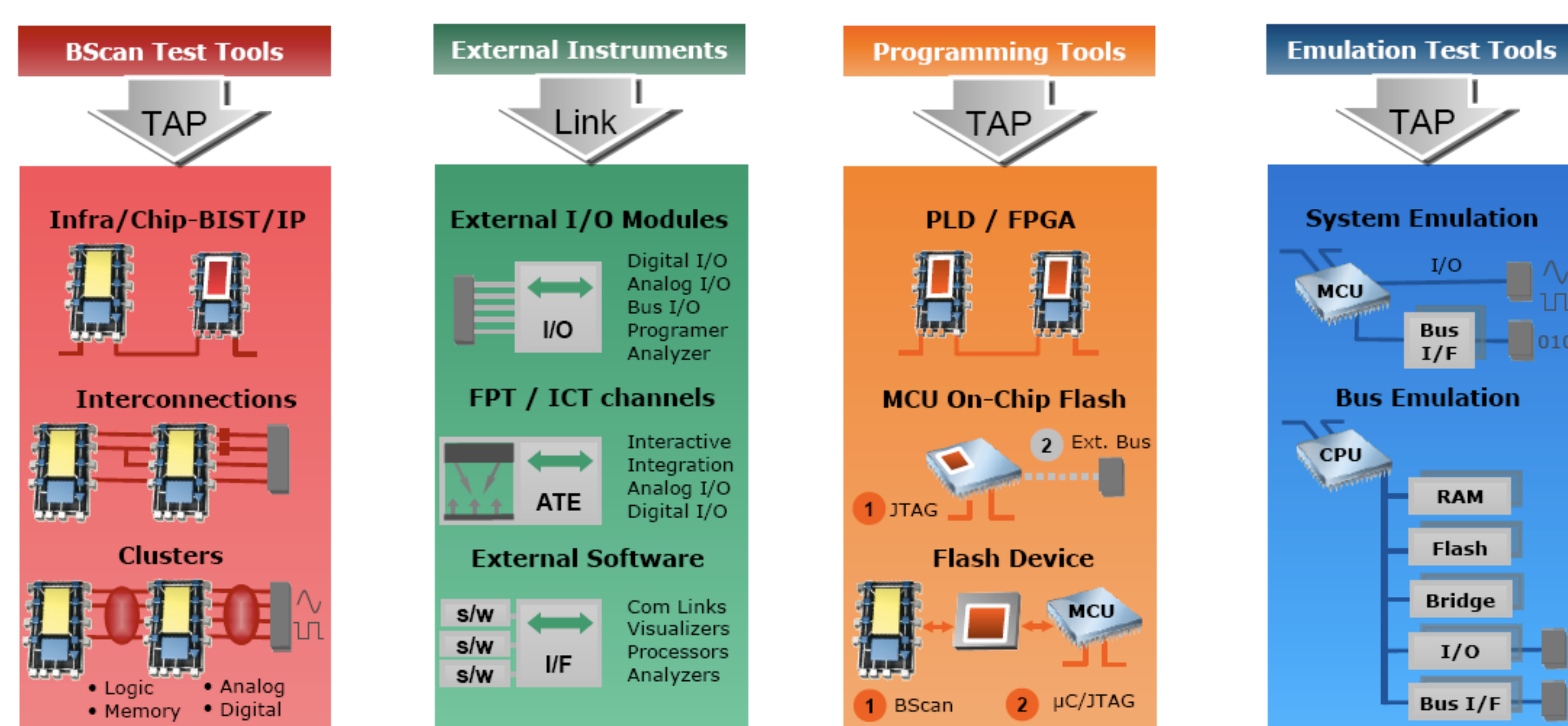


Classification of JTAG/Boundary Scan applications:

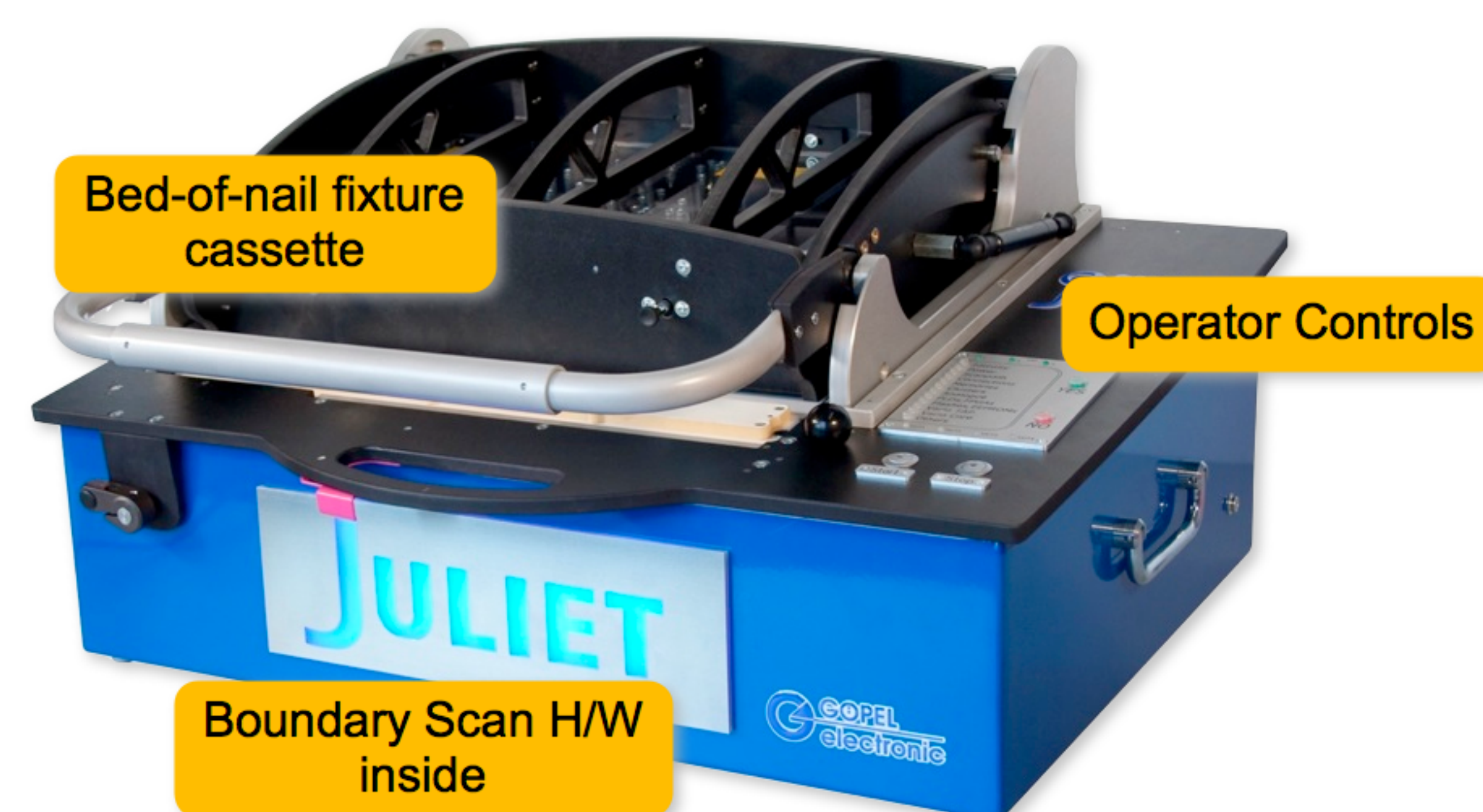


Frequent "Design For JTAG/Boundary Scan Test" (DFT) issues:

- TAP signals not accessible via connector
- Compliance Enable pins only accessible via test points
- Handling inefficiencies (too many cables to handle)
- Power Supply management
- Boundary Scan test coverage could be improved if test points of connector pins could be accessed with Tester I/O
- Overall test coverage could be improved by accessing analog circuitry with Tester resources

Universal, low-pin count ATE for PCA

... a solution to many Boundary Scan related DFT problems ...



- Integrated test/fixture electronics, power supply
- Bed-of-nail fixture / mass interconnect
- Compact, modular, JTAG/Boundary Scan based
- Interchangeable UUT adaptor
- Single UUT or Panel test

Example applications:

- Test and Programming of µP boards (BGA µP, RAM, Flash, ...)
- Test and Programming of boards with FPGA, PLDs
- Gang Programming of multiple boards (Flash Programming)
- VARIO TAP (Programming of internal Flash)
- Test of simple, non-scannable boards (Interface boards)
- Cable tester

and much more ...

Overview of common Test Methodologies:

Defect Type	AOI	AXI	ICT	FPT	FT	BScan
Visible Shorts	✓	✓ but not reasonable	✓	✓	✓	✓
Hidden Shorts	—	✓	✓	✓	✓	✓
Visible Opens	✓	✓ but not reasonable	✓	✓	✓	✓
Hidden Opens	—	difficult	✓	✓	✓	✓
Solder Quality	✓	✓	—	—	—	—
Missing Component	✓	✓	✓	✓	✓	partially
Wrong Component	partially	—	✓	✓	✓	partially
Orientation	✓	—	✓	✓	✓	✓
Misplaced / Alignment	✓	✓	—	—	—	—
Defective Component	—	—	✓	✓	✓	✓
Defective PCB	—	—	✓	✓	✓	✓
ESD / EMI	—	—	partially	partially	✓	partially
Design Problems	—	—	—	—	✓	partially
Software Defects	—	—	—	—	✓	partially
Benefit	Early in Process	X-Rays	Fast	No Fixture	Functional	Versatility
Disadvantage	No Electrical Test	Expensive	Requires Fixture	Slow	Expensive	Digital only*

Electrical Defects | Placement Errors | Soldering Defects