JTAG / BOUNDARY SCAN TUTORIAL
This White Paper introduces the reader to the Boundary Scan test methodology. Different Applications for Boundary Scan based on IEEE-Std. 1149.1 are discussed. An overview of related standards is provided in the second part of the document.
# Table of Contents

**JTAG / Boundary Scan Tutorial**  
Introduction  
The development of a new test methodology  
The JTAG / Boundary Scan Architecture  
The Boundary Scan Cells  
Test Bus Connection at Module- / Board-Level  
Hierarchical Test Bus Structures  
Built-In Self Test  
Test Tools  

**Test applications utilizing IEEE 1149.1**  
JTAG/Boundary Scan Infrastructure Test  
Interconnect Test  
Memory Access Test  
Logic Cluster Test  
In-System Programming of CPLD  
In-System Programming of EEPROM  
Built-In Self Test (Device Test / Emulation)  
Extended Interconnect Test  
Combined Boundary Scan - Functional Test  
Interlaced Emulation and Boundary Scan Test  

**Other standards related to IEEE 1149.1**  
IEEE 1149.4  
IEEE 1149.6  
IEEE 1500  
IEEE 1532  
IEEE P1581  
IEEE 1149.7  
IEEE P1687  

**GOEPEL Electronics**  

**Glossary**
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JTAG / Boundary Scan Tutorial

Introduction

Hardly any other test procedure has changed the testing grounds for manufacturers of electronic products the way In-Circuit Test did during the last 40 or so years. The reason for this triumph was that in-circuit testing is not confined to the test of the quality of the product but that it also shows the reasons for faults. Thus, the manufacturer has a tool that allows the creation of an automated quality control system. For example, if always the same faulty component were detected in a batch of boards, it would be recommendable to change the supplier. On the other hand, if the main reason for faulty boards is bad solder joints, the soldering process should be improved. Strictly speaking, one might think that the “philosopher’s stone” of Test had been found. This would be true – if it were not for the word “in-circuit”.

To test within a circuit is easier said than done, and it has not been possible without using bed-of-nail fixture technology. After some initial difficulties had been overcome, it was no problem to create the appropriate bed-of-nail fixture for any circuit - at least until the mid 1980s.

Soon, there were ideas about how the costs of test could be reduced by more universal approaches, e.g. by using the same bed-of-nail adapter for different test units. However, the technology of the component manufacturers rapidly developed, resulting in more and more gates placed onto the silicon die; nowadays entire systems are implemented within one integrated circuit. These systems still have to communicate with the environment, though, requiring the component to be equipped with pins. With drastically increased functional density of a circuit, the number of its pins inevitably has to rise, too. Sometimes simple laws of geometry become evident: room to put all necessary pins on the device package is getting scarce. The only way out is to reduce the space between the pins. So-called "fine-pitch packages" with a space of 0.3 mm between the pins are the standard today; technologies such as BGA (ball-grid-array) or those that completely dispense with the casing - such as COB (chip on board) – are used more and more. However, these new package technologies and the connection density that comes with them cause trouble for bed-of-nail fixture based testers. For if the raster of the connections gets narrower, then inevitably the probes of the bed-of-nails, too, have to be placed closer to each other. Yet, there are physical limits to this. Although, a possible way out of the dilemma, distributing test pads over the board is advantageous for the adaptation, it works against the purpose of saving space through highest integration. Here the idea of BOUNDARY SCAN comes in. Boundary Scan basically means to "get rid of the external test probe" (Fig.1). Boundary Scan is replacing the external probes of a test fixture with device-internal ones, the so-called "Electronic nails", being installed at the periphery of the functional silicon (on the device boundary).
The development of a new test methodology

To eliminate manufacturing faults, their sources have to be revealed. In order to achieve this, the stimulation and evaluation of the circuit nodes has proven to be effective. Manufacturers of integrated circuits pioneered the development of “scan procedures”. Well known is LSSD (Level Sensitive Scan Design) which was introduced by IBM in the 1960s. The basic idea is the division of digital circuits into combinatorial and sequential (typically flip-flops) circuit parts. The functional flip-flops are extended so that they can be used as shift registers in test mode. Test vectors can now be loaded into these shift registers and thus the flip-flops become access points to circuit nodes that can be stimulated and observed. The test of the combinatorial circuit parts can be executed through these circuit nodes, which are tested implicitly at the same time. As sequential logic is part of many integrated circuits, the test of peripheral circuitry had to be executed using external test resources rather than the shift registers mentioned above - until Boundary Scan was invented. It picks up the principle of flip-flops being connected to a shift register, yet this register is implemented into the silicon at the boundary of the circuit for the sole purpose of test access. For these flip-flops (Boundary Scan Cells) would impair the normal functioning of the circuit, they are connected to or disconnected from device pins and functional core via multiplexers. The basic functions of this architecture are:

- to capture test result vectors into the Boundary Scan cells,
- to serially shift in new test vectors and simultaneously shift out test result vectors that were captured,
- to apply a test vector previously shifted in to the circuitry to be tested,
- Test/stimulation of the inside of the integrated circuit (internal test), and
- Test/stimulation of outside signals being connected to the integrated circuit (external test).

An integrated circuit featuring this Boundary Scan capability has to be told which actions to carry out and it has to be synchronized with other Boundary Scan capable devices on the Unit Under Test (UUT). Thus, beside the actual test vectors it has to be provided with test instructions. For the purpose of providing the test instructions as well as test vectors and for synchronization between Boundary Scan capable components (short: BScan components) a test interface is required. In order to define such an interface and to standardize the Boundary Scan circuitry, a group of more than 200 members consisting of the leading manufacturers of integrated circuits, suppliers of test systems and manufacturers of electronic products came together to form the Joint European Test Action Group, later the Joint Test Action Group (JTAG). This group defined a four-wire test bus which optionally may be supplemented with a fifth test reset line. In order to make this test bus interface and the Boundary Scan test methodology a success as a platform which is independent from the manufacturer, it was proposed to the IEEE for standardization and eventually was approved as IEEE 1149.1 standard in 1990. Several extensions have been made since, with the latest having been approved in 2001. There has been work to complement the testability achieved by IEEE 1149.1. One working group developed an analog test bus interface for mixed signal test applications – standardized as IEEE 1149.4, approved in 1999. Another working group developed a multi drop test bus interface for test on system level, known as 1149.5 (although, this standard has not been adopted widely in the industry). The latest developments in high speed interconnects on board and system level initialized work on a test methodology for AC coupled and differential interconnects based on the 1149.1 test bus protocol. Work began in May 2001, was finalized in late 2002, with standardization as IEEE 1149.6 in January 2003. Newer IEEE standards related to IEEE 1149.1 include IEEE 1149.7 and IEEE 1581. And there are ongoing efforts today, extending the principles of IEEE 1149.1 to new applications and capabilities (e.g. IEEE P1838, IEEE P1149.8.1, IEEE P1687, SJTAG).
**The JTAG / Boundary Scan Architecture**

The fundamental components of the Boundary Scan architecture are the TAP (Test Access Port) and the Boundary Scan register made up of Boundary Scan Cells (Fig. 2).

The TAP is constructed as a finite state machine (Fig. 3) with 16 states. The transition from one state to another always occurs with the rising edge of TCK, with the level on TMS selecting the next state. The whole Boundary Scan structure must be implemented as synchronous design according to the standard. After power on of the device or after the TAP is forced into the reset state the Boundary Scan structure is inactive. Besides the Boundary Scan Register (BSR) an IEEE 1149.1 compliant device also contains an Instruction Register (IR) and a Bypass Register (BPR). The IR is used to define the test mode (e.g. Sample, Exttest, Bypass, etc.). The purpose of the BPR is to shorten the scan chain. Other optional data registers may be implemented, such as an Identification Register.

![Figure 2: Boundary Scan device](image2)

![Figure 3: Test Access Port (TAP) State Machine (as defined in IEEE 1149.1)](image3)
To distinguish whether data or an instruction is shifted, the TAP state machine has two separate paths featuring similar states (e.g. Scan DR / Scan IR). The states most essential for the test operation are the shifting of test data (Shift DR), the capturing of data into the register (Capture DR), the delivery of the test data to the output latches of the scan cells (Update DR) as well as the analogous states for the instruction register (Shift IR, Capture IR, Update IR).

As can be seen in Fig. 3, the transition from one state to another depends on the logic value on TMS. TMS (Test Mode Select) is one of the four signals that are also referred to as the Test Bus, or TAP interface, or JTAG pins. The TAP (Test Access Port) is a state machine synchronized by the Test Clock (TCK). The two other mandatory signals of the Test Bus are used for the test data transmission: Test Data In (TDI) and Test Data Out (TDO). /TRST (Test Reset, low active) is the only optional signal defined for the IEEE 1149.1 compliant Test Bus.

Beside the Boundary Scan Register (BSR), the standard specifies the existence of at least a Bypass Register (BPR) as additional data register. The BPR bypasses the BSR and thus shortens the scan chain by providing a 1 cell connection between TDI and TDO of the device. The data register between TDI and TDO of a device is selected by the instruction previously scanned into the Instruction Register.

The basic functions of the Boundary Scan architecture
1. Parallel capture of test result vectors into the Boundary Scan cells (capture)
2. Serial shifting in of test vectors and simultaneous shifting out of captured test results (shift)
3. Parallel connection of loaded test vectors to the circuit node that has to be tested (update)
4. Test / stimulation of the internal connections of an integrated circuit (internal test)
5. Test / stimulation of pin connections on a board- or system-level circuit (external test)

The Boundary Scan Cells

Boundary Scan cells are available in various types, their functionality depending on whether they are used for example to capture test results only (capture cells) or both to capture test results and to apply test stimulations. Fig. 4 shows examples of Boundary Scan cells: BC_1 is a unidirectional Scan cell used at inputs or outputs; BC_7 is a bidirectional scan cell. Details of cell type BC_1 are explained in the following.

The Capture Flip-Flop (FF) is clocked by the broadcast signal CLOCK_DR (from TAP controller) and captures data either from the previous scan cell (shift register mode) or the parallel input (pin or core logic). The shadow latch (or Update FF) takes over the data from the Capture FF after shifting, controlled by the broadcast signal UPDATE_DR (from TAP controller). The level of the MODE signal determines whether the value in the Update FF is transferred to the cell output (test mode) or not (operational mode).

Since the control signals (such as MODE, SHIFT_DR, UPDATE_DR and CLOCK_DR) are connected to all scan cells as broadcast signals, all cells within a Boundary Scan register are in the same mode at any given time. This means that all cells capable of capturing input data do so simultaneously with the rising edge on the CLOCK_DR in TAP state CAPTURE DR. Respectively, test data previously scanned into the cell is loaded in the Update FF and driven out with the falling edge on UPDATE_DR in TAP state UPDATE DR (for scan cells supporting that mode). Controlled by the signal MODE, and depending on the instruction loaded for the device (in the Instruction Register), all scan cells are either in functional mode (Parallel In connected to Parallel Out) or in test mode (Update FF connected to Parallel Out).
The Boundary Scan features implemented in a compliant device are described in a BSDL (Boundary Scan Description Language) file, which uses a subset of VHDL syntax. BSDL is defined as part of IEEE 1149.1.

### Overview of often used scan cell types
1. Universal cells with two multiplexers as well as capture- and shadow latch (supports capture and update)
2. Capture cells with one multiplexer and capture latch (supports only capture, e.g. as clock cell)
3. Update cell with one multiplexer, capture- and shadow latch (supports only the stimulation/update)
4. Checked output cells (the same as universal cells but samples Parallel Out rather than Parallel In)
5. Tri-State outputs (two-cell architecture for data output and disabling)
6. Bi-directional cell type A (two-cell architecture for disabling and data cell)
7. Bi-directional cell type B (three-cell architecture for disabling and data cells for input and output)
8. Internal cells with no connection to physical pin (typically update cells, e.g. for disabling)

### Standard instructions and often used optional instructions
1. Mandatory instruction BYPASS:
   - Bypass Register is put between TDI - TDO
   - Component is in functional mode
2. Mandatory instruction SAMPLE:
   - Boundary Scan Register is put between TDI - TDO
   - Component is in functional mode
3. Mandatory instruction PRELOAD:
   - Boundary Scan Register is put between TDI - TDO
   - Component is in functional mode
4. Mandatory instruction EXTEST:
   - Boundary Scan Register is put between TDI - TDO
   - Component is in test mode
5. Optional instruction IDCODE:
   - 32-bit Identification Register is put between TDI - TDO
   - Component is in functional mode

The Boundary Scan features implemented in a compliant device are described in a BSDL (Boundary Scan Description Language) file, which uses a subset of VHDL syntax. BSDL is defined as part of IEEE 1149.1.
Test Bus Connection at Module- / Board-Level

In order to use Boundary Scan at board or system level, the Test Access Ports of the involved devices need to be connected. This connection can be realized as:

- daisy chain configuration (Fig. 5);
- parallel / star configuration; or
- a mix of both.

In case the chain configuration is selected (most common), less space on the board is needed for signal routing as TDO and TDI are connected in serial. TCK and TMS are connected in parallel to all components involved.

In parallel/star configuration, individual scan chains are controlled by separate TMS and/or TCK signals. The advantage of this architecture is that in case there is a defective scan chain the others remain usable. However, the downside is the additional real estate on the board required for test signal routing. Therefore, the parallel/star architecture should only be chosen for very extensive designs or in case of special partitioning requirements. Special test bus routing devices (e.g. SCANBridge from National Semiconductors, or Scan Path Linker and Addressable Scan Port from Texas Instruments) are available for multi-drop and hierarchical scan chain designs, splitting a primary test bus into multiple secondary scan chains.

Hierarchical Test Bus Structures

One of the major advantages of Boundary Scan is that it simplifies system level interconnect test dramatically. Using this technology, connections between boards plugged into a backplane or between motherboard and daughter-cards can be verified easily. System level test often requires scan chain reconfiguration, though. Especially for backplane test, the test vectors have to be loaded into or read from the boards involved one at a time. Thus, the scan chains on these boards need to be addressable. Most of the time, system level Boundary Scan test requires a star configuration
of multiple scan chains (one or more scan chains on each board connected in parallel to the BScan controller). Thus, the BScan controller has to designate the test vectors sent to one of the scan chains. To do this, off-the-shelf addressable scan router devices are available as well as IP (Intellectual Property) cores for implementation into ASIC and PLD components. An example for a system level scan chain configuration is given in Fig. 6 below.

Figure 6: System-Level Scan Chain Configuration (SRD = Scan Router Device)

Process of a scan for the purpose of I/O interconnect test after power-on / reset:

1. Loading BScan instruction PRELOAD (preload function may be part of SAMPLE instruction) (addressing the Boundary Scan Register, keeps device in functional mode);
2. Preload safe values and the first test vector (simultaneous shifting out of contents of scan cells, to be disregarded);
3. Loading BScan instruction EXTEST (addressing the Boundary Scan Register, transition into test mode); The first test vector (previously loaded) appears at the output pins;
4. Transition to TAP state CAPTURE DR and then SHIFT DR;
5. The first response/result vector sampled at the input pins in CAPTURE DR is shifted out step by step (in SHIFT DR) clocked by TCK with TMS=0; simultaneously the second test vector is shifted in;
6. Transition to TAP state UPDATE DR;
7. The second test vector appears at the output pins with the falling TCK edge in UPDATE DR;
8. Repeat steps 4 through 7 for further test vectors (+ 1 last shift, in order to shift out the last result);
**Built-In Self Test**

Built-In Self Test becomes more popular these days, with device level implementations becoming more and more complex. SOC (System-On-Chip) applications implementing several CPU, DSP, Logic and Memory blocks on the same die are not uncommon today. To test these circuits efficiently, device internal test access is required. Furthermore, it becomes more and more important to test at least a few segments of modern circuits at speed. Boundary Scan does not provide for at-speed testing. However, the TAP defined in IEEE 1149.1 can be used to access internal test structures. Such internal test structures could be used to stimulate and/or observe parts of the circuitry implemented in an IC or they may even provide access to circuitry outside that device. A test utilizing these internal test structures is called a Built-In Self Test (BIST). Typically, the BIST circuitry is accessed through the TAP, initiated by a previously loaded BIST instruction. Fig. 7 below shows a sample implementation of BIST circuitry for on-chip memory and logic blocks.

![Figure 7: Access to Built-In Self Test (BIST) resources](image-url)
Test Tools

By now, most readers will agree that Boundary Scan is a powerful technology for mastering the test problems discussed in the introduction of this document. However, it is also clear that applying the Boundary Scan technique requires the command of the IEEE 1149.1 compliant test bus. It is not enough to provide test data or to read them out, but the TAP state machine has to be controlled as well. The attempt to control the TAP manually may well be successful; however, an effective test will hardly be possible. That is why tools relieving the user from the responsibility to control the Boundary Scan test bus and the TAP state machine have been introduced to the market very early. The user needs to focus on his test problem and he/she wants to describe test vectors the same way he/she has been used to with in-circuit or functional testers. Nowadays, the test program actually is generated automatically, based on CAD data. BSDL files provided by the device vendors provide the necessary information about the test features implemented in a Boundary Scan compliant device.

GÖPEL electronic has focused on these demands from the beginning, providing one of the most comprehensive, flexible, and user friendly Boundary Scan test systems available, known as SYSTEM CASCON.

In Boundary Scan test, software plays the most important role. Yet, the test methodology obviously requires hardware to apply the test vectors to the unit under test (UUT). GÖPEL electronic provides a broad portfolio of Boundary Scan controllers for PC based (PCI, PCI Express, USB, Fast-Ethernet, Firewire) as well as PXI, PXI Express, LXI, and VXI based test systems.

Test coverage and testability can be improved using external I/O modules that connect to otherwise not fully testable Boundary Scan nets on the UUT (e.g. through edge connectors). Here, GÖPEL electronic offers the widest selection of I/O modules and Boundary Scan accessories available on the market (e.g. CION modules, SCANFLEX I/O modules, and VarioCORE IP).

Boundary Scan test systems often are used as stand-alone tools. However, a combination of Boundary Scan with In-Circuit Test, Functional Test, Flying Probe Test and even Automated Optical Inspection systems may make sense as significantly higher fault coverage can be achieved.

The application of Boundary Scan is not limited to the board level. No other test procedure provides better possibilities for standardized, hierarchical test access than Boundary Scan, which can be used on component level, board level as well as on system level. Even remote test and diagnosis is possible.

However, not only testing is made easier or in same cases even made possible with Boundary Scan. Tasks that have nothing to do with testing can be simplified by utilizing the IEEE 1149.1 test access port. For instance, using the TAP to program PLD and FPGA devices and the Boundary Scan approach to program EEPROM devices soldered on the module/board is very popular.
IEEE 1149.1 can be utilized for a variety of test, debug, and in-system programming applications.

**JTAG/Boundary Scan Infrastructure Test**

Infrastructure (or Scan Chain Integrity) Test is used to ensure that the right BScan components are mounted and that the test resources and the scan chain(s) are accessible and functioning. This test verifies the Boundary Scan resources (register lengths and capture codes for ID-Code, Bypass, Instruction, and Boundary Scan Registers) of and the test bus connections between the various BScan devices on the UUT.

**Interconnect Test**

The Interconnect (or Interconnections, or Connectivity) Test verifies the connections between Boundary Scan pins. The existence of serial resistors and pull-resistors is verified as well as the function and connectivity of transparent clusters (e.g. buffer devices between BScan components). It includes test steps to find stuck-at-0 faults, stuck-at-1 faults, opens and shorts, and provides diagnostic information on BScan cell, pin and net level. During the Interconnect Test, Boundary Scan devices involved in the test are typically in EXTEST mode. The testability of a BScan net depends heavily on the boundary scan resources available in this net and on additional non-BScan pins connected to it. BScan nets featuring bi-directional BScan pins are tested in both directions, if possible.

The number of test vectors (scan cycles) generated depends on the number of BScan nets and on the highest number of BScan drivers found in any BScan net. Several test steps are generated: first stuck-at-low and stuck-at-high...
tests, then one or more “counter tests” to find shorts and opens. For stuck-at test, the maximum number of BScan
drivers in any one net is defining the total number of generated test vectors. For counter tests, the number of gener-
ated test vectors can be calculated per logarithm of the number of nets to the basis two. Specific UUT requirements
may increase or decrease the number of test vectors.

The Interconnect Test may include IEEE 1149.4 and IEEE 1149.6 compliant networks on the Unit Under Test.

**Memory Access Test**

A Memory Access (or Memory Cluster) Test verifies the connections between Boundary Scan pins and the memory
device (at the same time other BScan to BScan pin connections are checked as well). Existence of serial resistors
and pull-resistors is verified. The function of the memory devices and any logic between BScan device and the mem-
ory devices is also tested (although typically at slower speed than functional access).

- Access to all memory control pins is required (direct or indirect).
- Control over clock signals on SDRAM, and similar devices, is required.

**Logic Cluster Test**

A Logic Cluster Test verifies the connections from Boundary Scan pins to Cluster inputs and outputs and connections
within the cluster as well as the general cluster functionality. Fault isolation is limited due to missing Boundary Scan
access to all cluster-internal nodes.

- Keep logic clusters as small as possible.
- Control over non-BScan devices and clock signals (for sequential logic) is required.

**In-System Programming of CPLD**

Most modern programmable logic devices (PLD) provide a IEEE-1149.1 test bus interface and support in-system
programming (ISP) through that port. Typically, programming control is built in to the device and the control sequence
and programming data is provided by means of various file types, such as SVF files, JAM files, STAPL (Jedec-Std.
71) files, or IEEE 1532 files.

**In-System Programming of EEPROM**

Flash devices and other EEPROM (such as serial EEPROM based on I2C or SPI protocol) can be programmed via
Boundary Scan devices if access is available to all memory pins required for programming (either directly or indi-
rectly). To reduce programming time, a short scan chain and high TCK frequency are required.

- Separate the BScan device used to program EEPROM from other BScan devices (put it in a separate scan
  chain) if those devices support only a much slower TCK frequency.
- Try to control all EEPROM pins from the same BScan component (so that all other BScan components can be
  kept in HIGHZ, CLAMP, or BYPASS mode).
- Programming speed can be increased if frequently exercised control pins (such as /WE) are accessed with
  parallel I/O resources rather than Boundary Scan. Precondition for that is that the Boundary Scan pin in the
  respective net can be disabled and that access to the control pin is available via connector (preferably) or test
  pad.
**Built-In Self Test (Device Test / Emulation)**

Built-In Self Test (BIST) can be used to verify that a device is working properly after it has been assembled on a PCB. Usually, BIST is used to exercise device functions at speed. The test can be initiated via the IEEE-1149.1 test bus interface, e.g. by loading a BIST data register with stimulus applying the RUNBIST instruction. After completion, the test results (e.g. a signature pattern) can be read out via the test bus interface.

In a similar way, device emulation resources can be accessed through the test bus interface to debug device functions and/or firmware programmed into a device.

- Keep the device to be tested in a separate scan chain if the tool used to apply BIST pattern or emulation sequences cannot handle devices other than the target component in the same scan chain.

**Extended Interconnect Test**

Often times, Boundary Scan alone cannot test all of the board level circuitry completely. Usually, other test methodologies, such as MDA (Manufacturing Defect Analysis), AOI (Automatic Optical Inspection), ICT (In-Circuit Test), or FT (Functional Test), are used to complement Boundary Scan to achieve satisfactory test coverage. Executing all these tests in a separate step means board handling overhead that may be reduced by combining test methods.

Boundary Scan can be highly advantageous when integrated into ATE systems based on a bed-of-nails or moving probes (Flying Probe Testers). A combined solution can either reduce the number of nails required in a fixed-probe-adapter (thus dramatically reduce adapter cost), or it can improve the test time by reducing the number probing points required for an interconnect test based on moving probes.

**Combined Boundary Scan - Functional Test**

Combining Ad-Hoc test, such as FT (Functional Test), with Boundary Scan has the advantage, that functional test sequences become much simpler, since they don’t have to detect and locate/diagnose structural faults. Boundary Scan tests can be initiated at the beginning of the test sequence, verifying that there are no structural faults on the Unit Under Test (UUT) in the circuitry testable via Boundary Scan resources. After successful execution of the Boundary Scan tests, functional tests can be run to exercise the UUT at speed. Boundary Scan can be used to re-configure certain parts of the circuitry, e.g. to aid functional test or to load the firmware. At the most integrated level, both Boundary Scan resources and functional test resources can be used in conjunction to improve testability and simplify test sequences.

**Interlaced Emulation and Boundary Scan Test**

Introduced by GOEPBEL as part of the VarioTAP technology, Interlaced Emulation (and Boundary Scan) Test utilizes on-chip emulation resources accessible in many micro-processors (μP) and micro-controllers (μC) through an IEEE 1149.1 compatible JTAG Port, in conjunction with Boundary Scan registers in other devices on the Unit Under Test (UUT), in order to enhance the overall test coverage. Acting as an intelligent test controller at the functional core of the UUT, accessed via its JTAG port, the μP/μC generates dynamic test sequences that interact with Boundary Scan cells in other devices on the UUT (in an interlaced way), essentially providing virtual test points (virtual probes).

Supporting a real fusion of functional test via JTAG Emulation and structural test via Boundary Scan, VarioTAP redefines the concept of Extended JTAG/Boundary Scan, allowing the user to create procedures for:

- Structural test applications,
- Functional test applications,
- Structural functional test,
- Diagnostic test applications, and
- Custom applications

Figure 9: Extended test applications based on JTAG/Boundary Scan access, enabled by VarioTAP technology
Other standards related to IEEE 1149.1

IEEE 1149.1 provides a foundation other standards have been building on and ongoing standardization efforts continue to exploit and improve upon.

IEEE 1149.4

Approved in 1999, IEEE 1149.4 defines test resources and test access for mixed-signal Boundary Scan Test. The purpose of this standard is to provide the means to measure and characterize device level or board level mixed-signal and analogue parameters. IEEE 1149.4 compliant devices (which are also 1149.1 compliant) feature two additional test bus signals (AT1 and AT2). These two test bus signals can be connected to I/O pins through a switching structure (TBIC and ABM) for the purpose of test. Typically, they are used to provide a constant current to one pin and to measure the voltage on that and another pin. This test approach is used to measure resistance and capacities in the circuitry. Figure 11 provides a simple overview of what an IEEE 1149.4 compliant device could look like.
IEEE 1149.6

Work on a new standard (based on IEEE 1149.1) to test AC-coupled and other advanced I/O networks has been initiated in May 2001. Since Boundary Scan (IEEE 1149.1) provides for quasi-static structural test only, device, board or system level nets coupled through in-line capacitors cannot be tested with that approach. A more dynamic test circuitry was required to provide a high-speed signal that propagates through such AC coupled networks. The scope of work for the P1149.6 working group was to define Boundary Scan output cells and AC test signal generation as well as test receivers, and to specify the timing parameters required for a successful test of AC coupled networks. IEEE 1149.6, approved in 2003, defines the Boundary Scan structures and test instructions of compliant devices as well as the BSDL syntax used to describe these features. Figure 12 shows an implementation of a Boundary Scan output cell on a differential port with an AC selection cell. A sample implementation for an input Boundary Scan cell able to receive and analyze AC test signals is shown in Figure 13.

Figure 12: IEEE 1149.6 compliant Boundary Scan output cell on a differential driver

Figure 13: IEEE 1149.6 compliant Boundary Scan input cell on a differential receiver
IEEE 1500

This Standard for Embedded Core Test has been created to address the test complexity of System on Chips (SoCs) by providing a standardized test bus interface and a set of rules applied to isolate a particular core from the logic surrounding that core. The purpose of this isolation boundary (called a wrapper) is to allow the test of a core without any influence from circuitry outside the core, while keeping the amount of signals that must be brought out to the SoC level to a minimum. Similar to the Boundary Scan Register in a JTAG/Boundary Scan compliant device, the wrapper in a IEEE 1500 compliant devices comprises of wrapper cells for each functional I/O port. The wrapper cells are stringed together to form one or more wrapper scan chain(s). The wrapper cells are used to observe and stimulate the core logic they are linked to.

IEEE 1532

In-System Programming of PLD and FPGA is another application that utilizes the TAP defined in IEEE 1149.1. For years, different vendors of programmable devices had their own programming algorithms implemented in their device. Sometimes this caused problems when devices from different vendors where mixed within the same scan chain. With IEEE 1532 the programming algorithms for compliant devices as well as the format of programming data has been standardized for the first time. Thus, several devices (compliant with this standard) from different vendors within the same chain are now programmed using the same algorithms, simplifying programming tools and logistics. Furthermore, IEEE 1532-2002 defines the optional implementation of concurrent programming features. Concurrent programming can provide a significant improvement in programming time as more than one device can be programmed at the same time, rather than sequentially. Figure 14 outlines the principle of device programming via IEEE 1532.

Figure 14: IEEE 1532 for device programming
IEEE 1581

Today, IEEE 1149.1 test resources are implemented in many digital circuits (such as CPU’s, DSP’s, PLD/FPGA’s, interface devices, etc.). Even some memory components (e.g. some SRAM and FIFO components) have Boundary Scan implemented, although some of them do not support the EXTEST capability as defined in IEEE 1149.1. However, many Memory components do not have any test resources built in. The connectivity between Boundary Scan compliant components and such memory devices can only be tested by means of cluster testing (writing to the memory and reading back pattern written to the memory). This requires full access to the memory control pins, though. Many SDRAM or newer synchronous memory architectures are implemented on board level with clock circuitry that cannot be synchronized with Boundary Scan. This means that these memory structures cannot be tested via Boundary Scan in cluster tests. Today, no standard test methodology for memory testing is available. One approach introduced in the late 1990’s was SCITT. An IEEE working group (P1581) has been formed to create a standard test methodology for memory interconnect testing. In principle, IEEE Std 1581 describes test circuitry to be implemented in a memory device that bypasses the memory block itself and instead provides a logic connection between input and output pins (using simple logic gates). By stimulating the memory input pins and observing its output pins via BScan devices connected to the memory, board level connectivity can be verified; simplifying and accelerating this kind of test dramatically. The same technology can be applied to and implemented in other slave-type components.

IEEE Std 1581 has been approved in March 2011 and was published in June 2011.

![IEEE 1581 compliant device]

Figure 15: IEEE 1581 compliant device; test control via Test Mode Control logic or via optional Test Pin
IEEE 1149.7

The Mobile Industry Processor Interface (MIPI) Test and Debug Working group has selected a new test and debug interface, called Compact JTAG (cJTAG), which builds upon the IEEE Std. 1149.1 standard. The goal of cJTAG, standardized as IEEE 1149.7, is to enable advancements in test and debug functionality while maintaining compatibility with IEEE 1149.1 by creating a superset of the IEEE 1149.1 test interface.

A primary objective of cJTAG was to preserve the industry’s hardware and software investments in this standard. With cJTAG, existing tools or Debug and Test Systems (DTS), such as an IEEE 1149.1 emulator, and Target System (TS) chips, can simply be extended with adapters to convert to the cJTAG interface.

![Diagram](image)

Figure 16: IEEE 1149.7 introduces a narrow (two-pin) test bus interface as well as means to access a wide variety of chip-internal test, debug, and related functions [diagram from IEEE 1149.7 working group presentation]

Classes introduced and defined in IEEE 1149.7 introduce:

IEEE 1149.1 Extensions:
- Class **T0**: Assure IEEE Compliance for chips with multiple TAPs
- Class **T1**: Adding control functions (e.g. TAP power management, functional reset, etc.)
- Class **T2**: Adding performance features for series configurations
- Class **T3**: Adding performance features for star configurations

Advanced Two-Pin (test bus) Operation:
- Class **T4**: Adding two pin operation
- Class **T5**: Adding instruction/custom pin use to two pin operation
IEEE P1687

Also referred to as IJTAG (Internal JTAG), the IEEE P1687 working group intends to develop a methodology for access to embedded test and debug features (but not the features themselves) via the IEEE 1149.1 Test Access Port (TAP) and additional signals that may be required.

The IEEE 1149.1 standard specifies circuits to be embedded within an Integrated Circuit to support board test, namely the Test Access Port (TAP), TAP Controller, and a number of internal registers. In practice, the TAP and TAP controller are being used for other functions well beyond boundary scan in an ad-hoc manner across the industry to access a wide variety of internal chip test and debug features. The purpose of the IJTAG initiative is to provide an extension to the IEEE 1149.1 standard specifically aimed at using the TAP to manage the configuration, operation and collection of data from embedded test and debug circuitry. There exists the widespread use of embedded instrumentation (such as BIST Engines, Complex I/O Characterization and Calibration, Embedded Timing Instrumentation, etc.) each of which is accessed and managed by a variety of external instrumentation using a variety of mechanisms and protocols. Therefore, there exists a need for a standardization of these protocols in order to ensure an efficient and orderly methodology for the preparation of tests and the access and control of these embedded instruments. The elements of the methodology include a description language for the characteristics of the features and for communication with the features, and requirements for interfacing to the features. [Excerpt from the IEEE P1687 PAR]

![Figure 17: Examples of instruments implemented and accessible (via IEEE 1149.1 TAP) in an IEEE P1687](image)

IEEE P1687 focuses on:

- **Documentation**: architectural descriptions
  (identify accessible embedded instruments, specify characteristics of the instrument);
- **Access protocols**: procedure descriptions
  (how to communicate with an instrument, facilitate re-use through portability);
- **“Enhanced”**, secondary access/interface
  (Access instruments not easily handled solely by the TAP [i.e. use high bandwidth I/O], simplify hierarchical test architectures)
GOEPEL Electronics

GOEPEL electronics LLC is a subsidiary of GÖPEL electronic GmbH, headquartered in Jena, Germany. GÖPEL electronic GmbH was founded in 1991 as a spin-off of Carl Zeiss Jena and has several sales support offices in Germany, in France, in the UK, in Hong Kong, and in the USA.

The company is organized in three major business units:

- JTAG/Boundary Scan Systems
- Automotive Test and Functional Test Systems
- Automated Optical Inspection and Digital Image Processing Systems

GÖPEL was one of the world’s first suppliers of JTAG/Boundary Scan Test Equipment. From the beginning, the company has been setting pioneering trends to widely spread the use of JTAG/Boundary Scan standard IEEE 1149.1. Today GÖPEL is in a market leading position with thousands of installed systems in active use, offering mature software tools in an integrated development environment, high-performance Boundary Scan controllers and accessories, as well as comprehensive product support and value added services for IEEE 1149.x compliant test and in-system programming applications. GÖPEL electronic’s 170 skilled employees continually develop new and enhance existing products, generating a revenue of approximately EUR22 Million in 2010, while an extended distribution and service network of more than 300 specialists, including independent support centers, system integrators and value added resellers (VARs), ensures excellent local and on-site customer support world-wide.

Product and customer services are inseparable in GÖPEL’s business philosophy. As all products are provided from one source, hardware and software tools are optimally coordinated to allow system configurations that exactly match the required performance class.

The highest customer satisfaction and product quality is GÖPEL’s continuing goal. The company has continuously been ISO 9001 certified since 1996 and has been honored with TOP-JOB and TOP-100 awards for being one of the best medium-sized companies in Germany. GÖPEL electronic’s products have won several awards, including 2004, 2006, 2007, 2008, 2009, 2010, and 2011 “Best-in-Test Awards”, and are used by the leading companies in telecommunication, automotive, military, space and avionics, industrial controls, medical technology, and other industries.

For further information about GÖPEL electronic and our products and services please contact us or visit us on-line at www.goepel.com and at www.goepelusa.com.
Glossary

ABM
Analog Boundary Module

AC
Alternating Current

ADC
Analog to Digital Converter

AOI
Automated Optical Inspection

ASIC
Application-Specific Integrated Circuit

ATAP
Analog Test Access Port

ATE
Automated Test Equipment

AXI
Automated X-Ray Inspection

BGA
Ball-Grid Array

BERT
Bit Error Rate Test(er)

BIST
Built-In Self Test

BPR
Bypass Register

BSC
Boundary Scan Cell

BSR
Boundary Scan Register

BSDL
Boundary Scan Description Language

CAD
Computer Aided Design [Data]

CCA
Circuit Card Assembly

cJTAG
Compact JTAG

COB
Chip On Board

CPI
Central Processing Unit

CPLD
Complex PLD

DAC
Digital to Analog Converter

DC
Direct Current

DR
Data Register

DRAM
Dynamic RAM

DSP
Digital Signal Processor

DTS
Debug and Test System

EBST
Embedded Boundary Scan Test

EEPROM
Electrically Erasable Programmable Read-Only Memory

FF
Flip-Flop

FIFO
First-In / First-Out [Memory]

FPGA
Field-Programmable Gate Array

FPT
Flying Probe Test(er)

FT
Functional Test(er)

I2C
Inter-Integrated Circuit [Bus]

IEEE
Institute of Electrical and Electronics Engineers

IC
Integrated Circuit

ICE
In-Circuit Emulation

ICP
In-Circuit Programming

ICT
In-Circuit Test

I/F
Interface