Design for Testability and Extended Boundary Scan applications

Part 1 of a Webinar series presented by MJS Designs and GOEPEL Electronics
Your PCB electronics manufacturing services partner from engineering concept to prototype/production, since 1976

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Founded: 1991
Employees: ~ 160

JTAG / Boundary Scan,
Automotive Test Solutions, Functional Test,
AOI / AXI, Digital Image Processing
Outline

• Why do we need Design for Testability?
• Basics of JTAG / Boundary Scan
• Related IEEE standards
Why do we need DFT?
Why do we need DFT?

- Shrinking device geometries, device pitch
- New packaging technologies
- Diminishing test access
- Rising UUT complexity
- Rising test time

DFT = Design For Test / Testability
UUT = Unit Under Test
ITC = In-Circuit Test
Defect categories

- Design related defects
  - Design errors
  - Firmware / software errors
    - Simulation, Prototype (Design) Verification (DVT), HALT

- Electrically defective components
  - Bad components (e.g. due to ESD)
  - PCB / carrier with broken traces, etc.
    - Incoming inspection, QA at vendor

- Manufacturing related defects
  - Solder defects (Open, Short, etc.)
  - Misplaced or wrong components, etc.
    - Manufacturing Tests, HASS
Covering the “Defect Universe”

Test Coverage models for structural defects:

- **MPS** - Philips Research
  (Material, Placement, Solder)
- **PPVS** - ASTER Technologies
  (Presence, Polarity, Value, Solder)
- **PCOLA/SOQ** - Agilent Technologies
  (Presence, Correctness, Orientation, Live, Alignment, Short, Open, Quality)

Of concern for functional test coverage:

- Design defects
- Functional defects
Common manufacturing test solutions

AOI = Automated Optical Inspection
AXI = Automated X-Ray Inspection
FPT = Flying Probe Test
FT = Functional Test
ICT = In-Circuit Test
MDA = Manufacturing Defect Analyzer

AOI / AXI

FPT/ICT/MDA/Combination

Functional Test

Rework

Rework

Rework

Rework

AOI

Reflow

Screen Printing

Placement

Screen Printing

Placement

Screen Printing

Placement

Screen Printing

Placement
## Overview of Test Methodologies

<table>
<thead>
<tr>
<th>Defect Type</th>
<th>AOI</th>
<th>AXI</th>
<th>ICT</th>
<th>FPT</th>
<th>FT</th>
<th>BScan</th>
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<td>✓</td>
<td>✓</td>
<td>partially</td>
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<td>partially</td>
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<td>—</td>
<td>—</td>
<td>✓</td>
<td>partially</td>
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</tbody>
</table>

**Benefit**
- Early in Process
- X-Rays
- Fast
- No Fixture
- Functional
- Versatility

**Disadvantage**
- No Electrical Test
- Expensive
- Requires Fixture
- Slow
- Expensive
- Digital only*
Design For Test

Every test methodology requires some DFT

Balance test coverage and diagnostic capabilities with expected fault spectrum

Consider the cost of not testing or faults slipping through

Cost of test =

DFT + Test Development + Test Equipment
+ Maintenance + Test Time
+ Warranty for slip-through + ...
What is Boundary Scan?
What is Boundary Scan?

A little bit of history (and outlook) ...
IEEE 1149.1 specifies ...

- Test resources to be implemented in devices
- Boundary Scan

Description

Language (BSDL)
Boundary Scan / JTAG

- Regain test access (BGA, CSP, etc.)
- Quick test execution;
- Inexpensive test equipment;
- No or very simple test fixture;
BScan – PCOLA/SOQ

Component properties:
✓ Presence
✓ Correctness (correct device)
✓ Orientation
✓ Live (the device is *basically* alive)
  • Alignment
    (device is centered, no skews or small rotations)

Connections:
✓ Shorts
✓ Opens
  • Quality
Limits of Boundary Scan

- IEEE 1149.1 limited to digital interconnect test
- No at-speed test (exception: BIST)

New standards (IEEE 1149.4, 1149.6, ...)
Combination of Boundary Scan and other Test Methodologies
Basics of IEEE 1149.1

Mandatory features:
- Test Access Port (TAP): 
  - TCK, TMS, TDI, and TDO
- TAP Controller
- Instruction Register (2 bit or more)
- Bypass Register (1 bit)
- Boundary Scan Register (1 bit or more)

Instructions:
- BYPASS (opcode = all 1’s, perhaps others)
- SAMPLE
- PRELOAD
- EXTEST
Optional features:

- Fifth Test Access Port (TAP) signal: \(/TRST\)
- IDCode Register (32 bit)
- UserCode Register (32 bit)
- Other via TAP accessible resources
  (such as BIST circuitry, in-circuit programming controller, etc.)

Instructions:

- IDCODE
- USERCODE
- RUNBIST
- INTEST, CLAMP, HIGHZ
Linking multiple BScan devices

Scan Chain Design

- Daisy-chain (most common, shown below)
Extended Boundary Scan
IEEE 1149.1 in practice

Typical applications (only a few examples):

- Connectivity Tests; check for:
  - shorts between BScan accessible nets
  - opens on a BScan pin
  - stuck-at-0/1 faults at a net level
  - missing resistors
  - connections to memory devices
- Detect faults in non-BScan circuit clusters
- Control optical indicators (e.g. LED's)
- Provide easy test access for mixed-signal and functional tests
- Use SAMPLE mode to capture signal pattern
IEEE 1149.1 in practice

Detection / Diagnostics

OPEN  Yes / No
SA-0/1  Yes / Partial
SHORT Yes / Yes
IEEE 1149.1 in practice

Nets with at least three drivers and sensors (e.g. three bi-directional Boundary scan cells) allow full detection and diagnosis of Open, Stuck-at, and Bridging (Short) defects.

<table>
<thead>
<tr>
<th>Condition</th>
<th>YES / YES</th>
</tr>
</thead>
<tbody>
<tr>
<td>OPEN</td>
<td>Yes / Yes</td>
</tr>
<tr>
<td>SA-0/1</td>
<td>Yes / Yes</td>
</tr>
<tr>
<td>SHORT</td>
<td>Yes / Yes</td>
</tr>
</tbody>
</table>
IEEE 1149.1 in practice

How about non-BScan devices?
BScan Coach Software

Learn about IEEE 1149.1 device resources:
IEEE standards related to IEEE Std 1149.1
Basics of IEEE 1149.4

Parametric Test for

- Passive components (resistors, capacitors, inductors, etc.)
  and/or passive elements intrinsic to the interconnect
- Pull- or termination resistors
- Active components (diodes, transistors, sensors, etc.)
- Impedance networks

Extended Interconnect Test

- Limited number of devices available
- Ballot on BSDL Extensions expected in 2009, currently in ballot comment resolution
- Emerging tool support
Basics of IEEE 1149.4

Boundary Scan Cell

Internal Analog Test Bus

Core Logic (mixed signal)

BIST

TAP controller
Instruction Register and Decoder

AB
M

AB
M

AB
M

AT1
AT2

ATAP

TDI
TCK
TMS

TDO
Basics of IEEE 1149.4
Basics of IEEE 1149.6

- Extending IEEE-Std. 1149.1 capabilities by providing test methodology for
  - Differential interconnections
  - AC coupled networks
- Testing AC coupled networks with AC Test Signal
- Access to test resources through IEEE-1149.1 TAP
- Defines hardware structure and two new instructions
- Operates in parallel with IEEE 1149.1 and 1149.4
- Standard approved in 2003, tool support available
Signal coupling

Shown above are just a few sample coupling schemes.
Coupling capacities could also be implemented inside the IC.
1149.6 Main Features

A IEEE-1149.6 compliant device is also 1149.1 compliant

New AC-Test instructions defined in 1149.6:

- EXTEST_PULSE (mandatory)
- EXTEST_TRAIN (mandatory)

AC-pins receiving data have test receiver:

- Single ended AC-pin: one test receiver
- Differential channel: two test receiver

AC outputs use mission driver
Basics of IEEE 1532

- Standardized in-system programming (ISP) method
- Formal extension to IEEE-1149.1b-1994
- Access to on-chip programming resources via TAP
- Unified programming approach for devices from different vendors
- Concurrent programming of multiple devices from different vendors, reducing cost related to ISP
- Data and programming algorithm in separate files
New standards / initiatives

IEEE 1500
IEEE 1149.7 (cJTAG)
IEEE P1581
IEEE P1149.8.1 (BScan Selective Toggle)
IEEE P1687 (IJTAG)
SJTAG
Basics of IEEE P1581

To test connectivity to non-BScan devices easily

Solve test problems for devices such as DDR-SDRAM, DDR2-SDRAM, FLASH, etc.

- 1149.1 not built in!
- Controllability, complexity
- Test time
- Test conditions
  (use of untested resources to test the DUT)

Simple, quasi-static interconnect test
(no need for at-speed access or initialization)

Multiple P1581 devices in bus structure
Device is a “slave”

Test Control:
- Optional Test Pin, or
- Test Control Circuitry
P1581 test logic circuitry

- E.g. XOR/XNOR, or XOR/Inverters/AND
- Only combinational, non-sequential logic
- Easy to implement, simple test vectors
- Faults on pins don't inhibit test of other pins
- Fault detection guaranteed
- Fault diagnostics depends on implementation, test vectors
Basics of IEEE 1149.7

1149.7

- Narrow (2) or Wide (4)
- Debug/Test Framework

- JTAG
  - Boundary Scan
- Applications TAPs

- BDX
  - Bulk Data Transfer
  - Instrumentation Sources

- CDX
  - Custom Data Transfer
  - BDM (Freescale)/ SWD (ARM)/other

- Power
  - Power down test logic when not used

- Test
  - Test and Private Interface Modes
Classes of IEEE 1149.7

Class **T0**
Assure IEEE 1149.1 compliance for chips with multiple TAPs

Class **T1**
Adding control functions (e.g. TAP power management)

Class **T2**
Adding performance features for series configurations

Class **T3**
Adding performance features for star configurations

Class **T4**
Adding two pin operation

Class **T5**
Adding instruction/custom pin use to two pin operation

Legacy Capability (IEEE 1149.1 compliant)

Extended Capability

Advanced Capability (two-pin operation)
Focus on

**Documentation**: architectural descriptions
- Identify accessible embedded instruments,
- Specify characteristics of the instrument;

**Access protocols**: procedure descriptions
- How to communicate with an instrument,
- Facilitate re-use through portability;

“Enhanced”, secondary access/interface:
- Access instruments not easily handled solely by the TAP (i.e. use high bandwidth I/O)
- Simplify hierarchical test architectures
Basics of SJTAG

Goal:

to standardize data contents and formats for communication:

between external Test Manager platforms and internal Embedded Test Controllers,

and

between Embedded Test Controllers and the UUTs they serve

for all variants of XBST and EBST

XBST - external Boundary Scan Test
EBST - embedded Boundary Scan Test
References and Contact Information
References

Books:

References

Websites:
- www.goepel-genesis.com
- www.goepel.com
- www.DFTguide.com
- www.DFTdigest.com

Other publications:
- ITC Proceedings (papers on the topic; there are plenty ...)
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