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TAP Checker™ — EDA software to verify BSDL files

This innovative tool suite enables the automatic generation of simulation vectors and test patterns for chip-level validation and verification of IEEE 1149.1 and IEEE 1149.6 compliant implementation. TAP Checker is based on a modular platform architecture with a central database and individually licensed modules for data import, automatic test vector generation and data export. This structure enables a scalable tool suite that can also support new bus protocols without losing backward compatibility. After importing the Boundary-Scan Description Language (BSDL) file, a process which includes syntax, semantics, and consistency verification, the user has a multitude of parametrized options, providing the means to generate an optimized testbench.

TAP Checker highlights

- Automated Test Bench Generation for Validation and Verification of JTAG/Boundary Scan Designs, including BSDL syntax and semantics verification
- Support for multi-chip modules and 3-D ICs
- GUI and command line
- Output formats:
  - ✓ Verilog (IEEE 1364)
  - ✓ VHDL (IEEE 1076)
  - ✓ STIL (IEEE 1450)

JTAG Boundary Scan IEEE 1149.x

Contact us for more information:
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TAP Checker™ is a new generation EDA software tool for verification of Boundary Scan Description Language) BSDL files and validation of JTAG implementations in integrated circuits. The innovative tool suite enables the automatic generation of simulation vectors and test patterns for chip-level validation and verification of IEEE 1149.1 and IEEE 1149.6 implementation. The TAP Checker™ tool is well positioned to support future IEEE test and debug standards due to its modular architecture. The quality of BSDL files has a fundamental impact on the efficiency of project development for all JTAG/Boundary Scan test and programming applications.

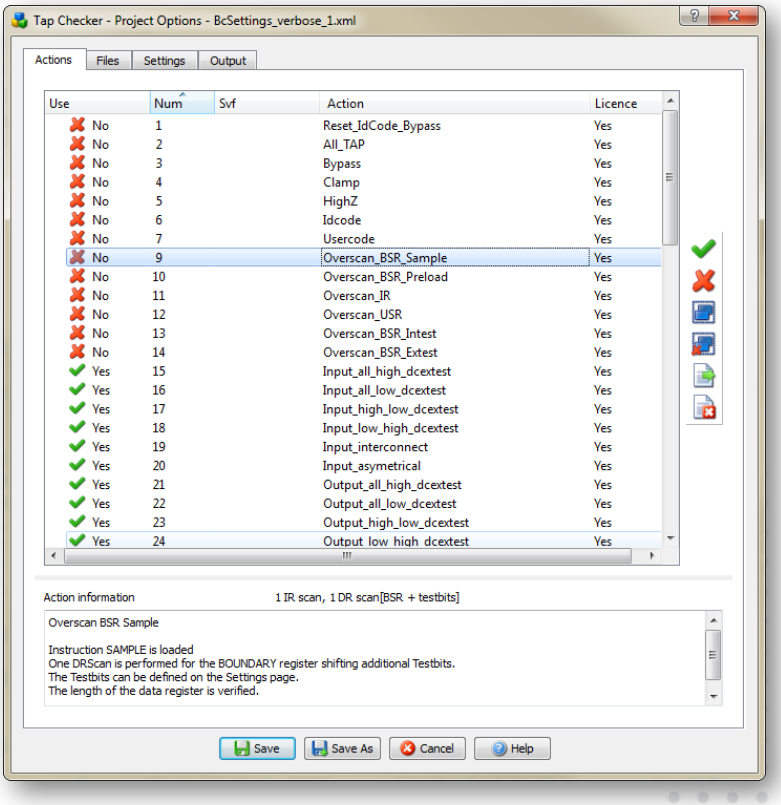

Figure 1: Test step selection

As a spin-off of an already industry-proven Computer Aided Test (CAT) software suite, TAP Checker benefits tremendously from existing experience and infrastructure. This strategy also provides for an excellent synergy between chip and board level system test solutions. This new software generation is also well positioned to tackle future technology driven changes in standards related to test and debug. TAP Checker™ is based on a modular platform architecture with a central database and individually licensed modules for data import, automatic test vector generation and data export. This structure enables a scalable tool suite that can also support new bus protocols without losing backward compatibility. After importing the BSDL file, a process which includes syntax, semantics, and consistency verification, the user has a multitude of parametrized options, providing the means to generate an optimized testbench. In addition to IEEE 1149.1, TAP Checker™ also supports IEEE 1149.6 for the test of advanced digital networks. For all operations the tool can insert customer-specific initialization and control sequences in the testbench, significantly improving flexibility. Options for VHDL (IEEE 1076), Verilog (IEEE 1364) and STIL (IEEE 1450) are available for testbench and test pattern export. As a result the TAP Checker™ outputs can not only be used in any simulators but can be transferred to all market-leading chip testers through STIL (a standardized test vector format), helping to improve testbench quality and to increase fault coverage in semiconductor test.

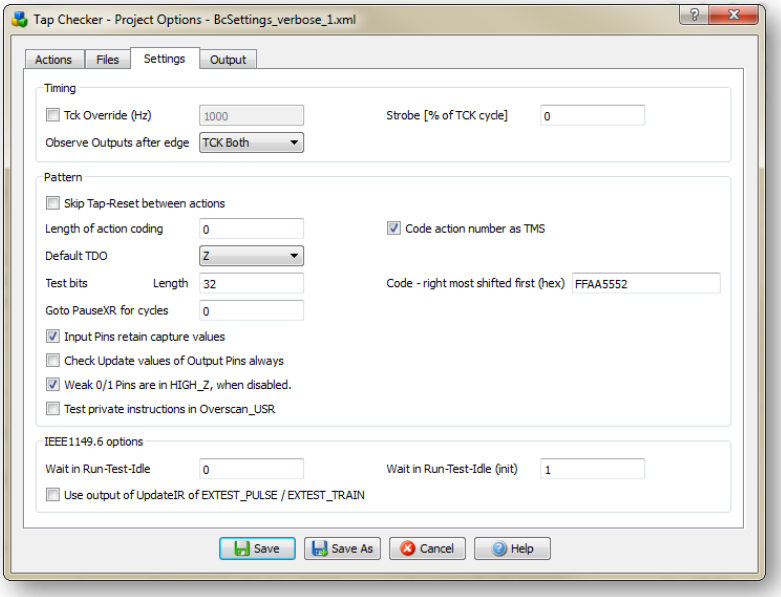

Figure 2: Project settings

TAP Checker™ is shipping and is available for SOLARIS™, Windows® and LINUX operating systems.

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