JTAG / boundary scan tools by GOEPEL electronics

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What is JTAG / boundary scan ?

JTAG / boundary scan was the first test methodology to become an IEEE standard. The standard number is IEEE 1149.1 and its initial version was balloted on and approved in 1990. This standard defines features to be designed into an integrated circuit that provides access to its digital I/O pins from the inside of the device. This allows circuit nodes on the PCB to be accessed with device internal test features, rather than with a bed-of-nails fixture or with moving probes. (GOEPEL offers a software tool explaining IEEE 1149.1 features and their functions. It is available free of charge upon request.) With these built-in test features, boundary scan helps us to access circuit nodes that may not be accessible when using external physical access methods with probes. This is especially important when considering the wide use of high-density device packages and components with hidden solder joints (such as BGA, micro BGA, and so on). Boundary scan also has the potential to shorten time-to-market since it can be used very early in the product life cycle, potentially without the need for any bed-of-nails fixture or flying probes.

Furthermore, boundary scan can be used throughout the whole product life cycle, since test vectors can be applied with very simple test equipment. Special circuitry to execute boundary scan tests can even be embedded on a Printed Circuit Assembly for use at the system level, for example as part of power-on self tests for systems out in the field. Boundary scan tests can be developed very rapidly and early in the design cycle, typically as soon as a schematic design of the UUT is available, even prior to having the layout of the PCB finished.

The primary application, for which boundary scan was initially developed, was to detect and diagnose manufacturing defects related to connectivity at the board level, such as stuck-at-0 and stuck-at-1 faults, open solder joints, and shorted circuit nodes. Today, the test access port defined in IEEE 1149.1 is used for many additional applications, such as in-system programming, access to built-in self test, on-chip emulation and debug resources, and system level test.

JTAG stands for Joint Test Action Group, which was a group of interested parties that set out to develop the test methodology that became IEEE 1149.1. Since then, many standard development efforts built on the original work by reusing features defined in 1149.1. One such standard is IEEE 1149.4, which defines device features supporting the test of analog circuits. Another example is IEEE 1149.6, which defines test resources used to verify AC-coupled networks, improving testability of technologies such as differential networks. IEEE 1532 defines in-system programming features accessible via the test access port defined in 1149.1, essentially providing a common method to program devices from different vendors. A number of additional standardization efforts related to JTAG / boundary scan have recently been completed (e.g. IEEE 1149.7, IEEE 1500) or are under

way (e.g. IEEE P1149.8.1, IEEE P1581, IEEE P1687, SJTAG).

GOEPEL can provide Design for Testability guidelines and even offers DFT analysis for boundary scan free of charge.

We also offer a variety of seminars and training programs covering boundary scan technology and GOEPEL boundary scan tools. Seminars are offered as half day and full day events, training classes last from one day to four days, depending on the curriculum. Both seminars and training classes can be customized to cover specific topics and can be provided on-site for a corporate audience. We also offer web based training through webinars and conference calls.
For a schedule of upcoming webinars, seminars, and training classes, visit our events page. Or contact us to request further information.

Overview of JTAG / boundary scan tools offered by GOEPEL

Most boundary scan testers are PC based test systems. Sometimes, however, boundary scan tools are integrated and combined with other automated test equipment (such as bed-of-nail based in-circuit testers, flying probe testers, or functional testers). In general, boundary scan software is used to generate the test pattern, to apply the test vectors to the Unit Under Test (UUT), and to analyze the response vectors from the UUT. Test vectors are delivered to the UUT with a boundary scan controller and some form of Test Access Port (TAP) interface. Boundary scan controllers are available for a wide variety of hardware platforms such as PCI, PXI, VXI, PCI Express and PXI Express as well as for USB, LAN, LXI and other bus interfaces. The TAP interface hardware is connected to the UUT's test bus connectors, providing access to the key TAP signals, TCK, TMS, TDI, TDO, and /TRST. TAP interface hardware may provide a number of TAP's for connection to multiple scan chains, as well as additional test resources such as digital and analog I/O. JTAG / boundary scan requires the UUT to be powered-up, so the tester setup also needs to include a power supply for the UUT. And finally, a test system may provide additional boundary scan I/O channels and other digital and mixed-signal I/O for the verification of UUT interfaces in order to extend the test coverage achievable with boundary scan on a particular UUT. Such I/O modules are available in a variety of form factors and feature sets.

GOEPEL offers the most comprehensive and technologically advanced JTAG / boundary scan software and hardware tools in the industry.

The quality of a JTAG/boundary scan systems is primarily defined by the performance and the architecture of its software. In 1991, GOEPEL electronic was the worldwide first vendor to introduce a specialized software technology in form of an Integrated JTAG/boundary scan Development Environment (IDE) - SYSTEM CASCON™ was born. The uniqueness of this JTAG/boundary scan Workbench has been maintained over the years through continuous integration of new, intelligent tools paired with innovative system extensions and improvements in the user interface.

SYSTEM CASCON™ is an open, graphical JTAG/boundary scan operating system and programming environment. Its architecture thoroughly implements GOEPEL Electronic's philosophy of Extended JTAG/boundary scan, eclipsing other solutions with regard to test coverage and system functionality by combining various test, programming and emulation methods with native JTAG/ boundary scan procedures.

The completely integrated architecture of SYSTEM CASCON™ provides the flexibility needed to adapt the software configuration to completely different target applications and environments. Software packages designed for laboratory, production, and field service are available in various performance classes (Editions) as Development Stations (DS) and Test/Execution Stations (TS/ES), and individual tools can be added or removed from software package licenses. Pure in-system programming (ISP) applications can be realized with CASCON POLARIS™ Editions, while CASCON GALAXY® supports both ISP and test applications. The extensive CASCON Application Programming Interface (CAPI) enables powerful integrations. As an alternative to node-locked licenses, floating licenses provide efficiency with multi-seat and multi-tooling capabilities.

A boundary scan controller provides the hardware interface between tester and Unit Under Test (UUT). GOEPEL offers the widest product range supporting test and ISP applications throughout the UUT's product life cycle. The choice of controller hardware depends on particular application requirements. Test programs created with SYSTEM CASCON software (CASCON GALAXY®, CASCON POLARIS™) are cross compatible with all GOEPEL boundary scan controllers.

With SCANFLEX®, GOEPEL has developed a hardware architecture that is unique and unmatched in modularity, flexibility, and feature set.

The SCANBOOSTER™ controller family offers a low price alternative for applications where the advanced features of SCANFLEX® are not required, while still offering multiple TAPs as well as 32 parallel I/O port (PIP) signals.

We also offer low-cost boundary scan solutions that bundle a CASCON GALAXY software package with SCANBOOSTER hardware. These bundles have been created for design, production and service personnel looking for a fast turnaround in terms of application development at a very low cost.

In addition, GOEPEL offers a wide variety of hardware accessories, including I/O modules (for standard interfaces, such as DIMM or PCI or PCIe, for example, as well as for custom interfaces and for fixture integration) and adapter solutions for prototyping and low-volume production test.

Use this [feedback form] to specify your requirements for a JTAG tool set and we'll get back to you with a customized proposal - "no strings attached".

Please contact us to request further information.

Questions to consider when choosing a JTAG / boundary scan system

Unit Under Test related questions:

- Do you have a CPU, CPLD, FPGA, or other complex devices and/or components in high density packages such as BGA, microBGA on your board?
- What type of non-boundary scan devices does the Unit Under Test (UUT) feature (e.g. Static Memory [SRAM], Dynamic Memory [SDRAM, DDR SDRAM, ...], NOR Flash, NAND Flash, serial EEPROM, discrete logic devices [e.g. 74LVT00] or Decoders, peripheral connectors with many digital signals, and/or DIMM sockets)?
- When/where in the UUT's product life cycle do you intend to use JTAG/boundary scan?

Software related questions:

- For what purpose do you intend to implement this JTAG / boundary scan system: Design Validation and Prototype Verification, Manufacturing Test, Repair and Troubleshooting, Field Service, or for some other purpose?
- Do you intend to develop your own JTAG/boundary scan applications, or would you outsource the test development?
- Would this station be intended for boundary scan test only or would you want to test your products and also program CPLD or Flash devices or serial EEPROMs?
- What are the primary types of JTAG / boundary scan applications you are interested in? For example: Connectivity Tests (finding manufacturing faults, such as opens, shorts, stuck-at faults), In-System Programming for CPLD / FPGA devices, In-System Programming for serial EEPROM and/or Flash devices, In-System programming of On-Chip Memory (e.g. Flash memory inside a CPU, DSP, or Micro-Controller), Utilize On-Chip Emulation for structural tests and for JTAG controlled functional tests, some other application?
- What should this software package allow me to do? For example: Develop JTAG / boundary scan applications, Generate tests automatically, Write tests manually in a scripting language, Execute test and In-System Programming routines, Generate detailed pin and net level diagnostic messages in case of detected defects, Debug JTAG / boundary scan applications, Present the Layout and/or Schematic view of the Unit Under Test.
- Would you prefer a node-locked license (USB dongle) or a floating (network) license? In case of a network license, would you want to share the license with other facilities in the country or even globally?

Hardware related questions:

- How would you like to connect the JTAG / boundary scan controller hardware to the tester PC: USB, PCI, PXI, Ethernet, PCI Express, PXI Express, LXI, Cabled PCI Express, some other bus?
- How many scan chains do your UUTs typically have?
- How many scan chains do you need to control concurrently?
- Do you intend to test/program multiple UUTs at the same time (concurrently) with this test system?

- What is the maximum TCK frequency the boundary scan devices on your UUTs typically support?
- Would this station be intended for boundary scan test only or would you also want to program Flash devices or serial EEPROMs?
- Have you experienced or expect to experience any Design for Test (DFT) issues related to JTAG / boundary scan, such as a Scan Chain that is not designed properly, TAP signals on JTAG compliant devices that are only accessible through test points, Compliance Enable conditions that can only be satisfied by probing test points, or some other DFT problems?
- Do you need tester I/O channels in order to include peripheral I/O connectors on the UUT in the boundary scan tests?
- Do you intend to run the JTAG/boundary scan system as a stand-alone installation or would you want to integrate the tools in third-party ATE equipment (such as In-Circuit Tester, Flying-Probe Tester, Functional Tester)?

Services related questions:

- Are you interested in a DFT Analysis on one of your UUTs? Will you require system and/or test technology training?
- Are you interested in our test development services, BSDL Verification Services, and/or turn-key solutions?

Please contact us to request further information.

[more about GOEPEL boundary scan]