Introduction to JTAG / Boundary Scan

Introduction to JTAG / Boundary Scan

- One **half-day** course: 10am through 2pm in Austin, TX
- Introduction to JTAG / Boundary Scan / IEEE 1149.1 and related technology
- Design for Testability guidelines related to JTAG / Boundary Scan
- Demonstration of software used to develop, execute, and debug JTAG/Boundary Scan applications
- Lunch provided
- Recommended for design, test, and production engineers and managers

Outline

Morning:

- What is JTAG/Boundary Scan? (some history, technology background, current developments in the industry)
- Boundary Scan applications (types of tests, in-system programming, board level vs. system level)
- Design for Test for JTAG/Boundary Scan (device and board requirements)
- How to analyze a Unit Under Test to identify possible applications with Boundary Scan
- General test development flow

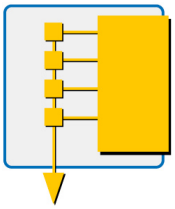
Lunch break

Afternoon:

- Demonstration of SYSTEM CASCON (Integrated development tool suite for JTAG/Boundary Scan applications)
  - Project transfer
  - CAD Import, Netlist Merging
  - Device Classification and Model assignment
  - Navigation between different tools in SYSTEM CASCON
  - Test development and Execution
  - In-System Programming
  - Test Coverage Analyzer
  - ScanAssist Debugger - overview

Free of charge

See schedule at **www.goepelusa.com/events**
Contact us to register:
888-4-GOEPEL OR 512-524-6063
or email us at sales@goepelusa.com



Introduction to SYSTEM CASCON

- **Full-day** course: 8am through 4pm, at GOEPEL Training facility in Austin, TX
- Introduction to JTAG / Boundary Scan / IEEE 1149.1 and related technology
- Design for Testability guidelines related to JTAG / Boundary Scan
- Hands-on: Learn how to use SYSTEM CASCON to develop, execute, and debug JTAG/Boundary Scan applications
- Lunch provided
- Recommended for design and test engineers

Outline

Morning:

- What is JTAG/Boundary Scan? (some history, technology background, current developments in the industry)
- JTAG / Boundary Scan applications
  (types of tests, in-system programming, device emulation, board level vs. system level)
- Design for Test for JTAG/Boundary Scan (device and board requirements)
- How to analyze a Unit Under Test to identify possible applications with Boundary Scan
- Overview of SYSTEM CASCON
- General test development flow

Afternoon:

- **Hands-on exercises** with SYSTEM CASCON software
  (Integrated development tool suite for JTAG/Boundary Scan applications)
  - Project transfer
  - CAD Import, Netlist Merging
  - Device Classification and Model assignment
  - Navigation between different tools in SYSTEM CASCON
  - Generating and executing Infrastructure Test
  - Generating and executing Interconnect Test
  - Generating and executing Memory Access Test
  - Generating and executing Logic Cluster Test
  - FLASH programming
  - PLD Programming
  - Test Coverage Analyzer
  - ScanAssist Debugger and PinToggler
  - CASCON Batch sequence
  - Project archiving

Class size is limited to 6 students
to ensure a high-quality learning experience

Product: CASCON Intro
Part Number: TRB-110

US$299 per student

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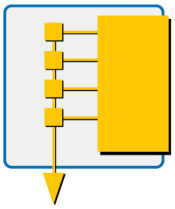

Introduction to SYSTEM CASCON